Digital Generation of RF Signals for Wireless Communications With Band-Pass Delta-Sigma Modulation

J. Keyzer, J. Hinrichs, A. Metzger, M. Iwamoto, I. Galton, and P. Asbeck

University of California, San Diego, La Jolla, CA 92093-0407

ABSTRACT — **This paper demonstrates a high speed digital technique to produce binary (digital) signals that encode representative RF signals (with time varying envelope) as needed for wireless communications. Specifically, it shows that IS-95 format CDMA signals can be generated with a single bit digital data stream at 3.6Gb/S. The technique uses band-pass delta-sigma modulation so that the quantization noise is shaped out of the frequency band of interest. This approach points the way to single-chip, DSP-based transmitters, used in conjunction with switching mode power amplifiers and simple analog filters, to implement all the functions of a wireless transmitter.**

I. INTRODUCTION

As CMOS-based DSP performance increases and its cost in terms of power dissipation and circuit area drops, there is increasing opportunity to implement RF functions with DSP. According to the ITRS Roadmap, the clock rate of high performance chips will reach 3.5 GHz in 2005. This implies that CMOS will have a significant role in microwave functions, not just as analog-based "RF CMOS", but in the form of digital circuits.

DSP based systems potentially can provide many benefits for an RF transmitter: no tuning requirements, no aging problems, higher integration and smaller size, easier test, and, potentially, much greater flexibility and programmability. If "mostly-CMOS" RF transmitters can be realized, there are numerous opportunities for innovation in the areas of architectures, circuit functions and signal formats. Complicated modulation approaches can be implemented, and changed as needed via straightforward reconfiguration of the DSP. With appropriate sensors for feedback, the DSP can also be made to adapt to impairments of components and the RF channel.

One of the stumbling blocks for digital transmitters and receivers is the need for high-speed digital-to-analog converters with high resolution and very high speed. This problem potentially can be circumvented with the use of low-resolution converters (potentially down to 1 bit converters, which are inherently linear). In this work, we show that band-pass delta-sigma algorithms are promising to achieve microwave signals using clocked binary signals (digital data streams) with good fidelity over a specified frequency band. We demonstrate the results experimentally with the generation of 1 bit digital data streams which, over a specified frequency band, are capable of meeting the requirements for CDMA systems (IS-95).

II. SIGNAL GENERATION APPROACH

Transmitters implemented with analog and RF electronics typically include a variety of functions. In many cases, the in-phase (I) and quadrature (Q) baseband signals, are computed at baseband frequencies with digital signal processing (DSP), and subsequently converted to the analog domain with digital-to-analog converters (DACs) of moderate resolution (4-12 bits). The signals are subsequently upconverted to RF, often via an intermediate frequency stage, using quadrature mixers and filters. A variable gain stage is often included. Finally, the transmitter comprises a power amplifier and an output coupler.

In this paper we demonstrate an alternative architecture, which potentially is easier to implement. There is no need for a high resolution D/A converter if the resulting signal is encoded in a suitable band-pass delta-sigma (BPDS) format, in which case a single bit D/A converter is sufficient. Moreover it has been shown recently that RF power amplifiers driven by such BPDS signals can attain high efficiency, together with good linearity, as required for many communication formats, such as QPSK [1-3]. The high efficiency results from the fact that switching mode amplifiers can be used, in which the transistors are either fully on or fully off during as much of the RF cycle as possible, and, as a result, their internal power dissipation is minimized. The power amplifier driven with the BPDS signals, however must be followed by an analog filter, to remove out of band quantization noise.

Transmitter Architecture: The proposed architecture is shown in Fig. 1. The DSP computes a BPDS encoded, upconverted version of the signals contained in the I and Q digital data streams. The DSP is carried out with various stages. The final stage operates with the highest clock rate, f_s. For a desired output carrier frequency f_o, the clock rate f_s is selected to correspond to a multiple of f_o (typically $fs=4f_o$) in order to simplify the computations. To generate

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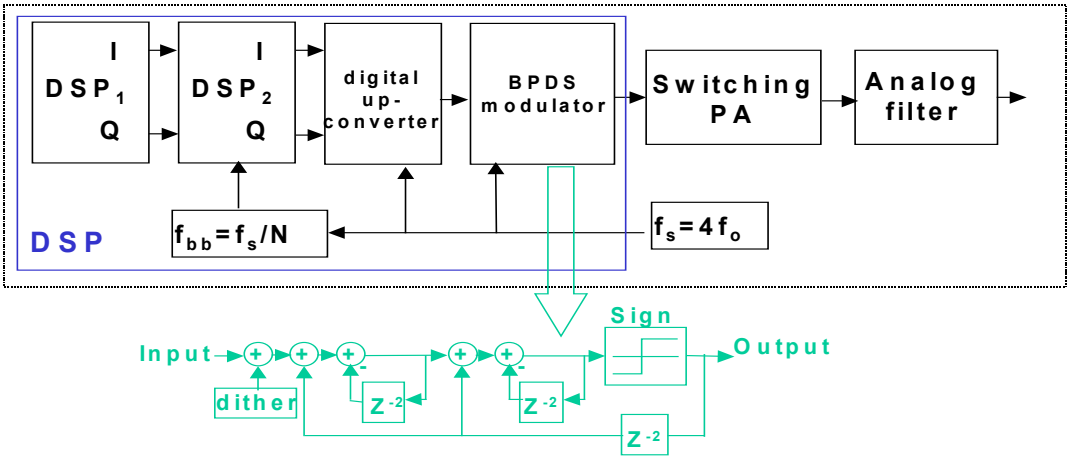

Fig. 1: Schematic diagram of transmitter architecture. Representative implementation of the band-pass delta-sigma modulator is shown.

signals with different carrier frequencies, a phase locked loop with frequency control to generate f_s is assumed. Such a variable frequency source is used in conventional RF transmitters, only in the present case, instead of mixing with the signal, this frequency provides the DSP clock. Inasmuch as the DSP used to generate the I and Q signals at baseband does not operate with a clock that is compatible with the high frequency output clock f_s, a conversion of clock rates must be carried out. This is accomplished most easily at the lowest possible clock rates (the baseband portion of the transmitter).

Ideally, an upconversion stage implements the operation

$$y(t)= x_i(t) \sin(2\pi f_o t) + x_q(t) \cos(2\pi f_o t) \qquad (1)$$

where $x_i(t)$ and $x_q(t)$ are the analog I and Q channel signals. In the proposed transmitter, the I and Q signals are provided by samples at a frequency f_{bb} which is an exact submultiple of f_s, and which typically is chosen to be higher than the desired signal bandwidth by a factor of at least 10 (with moderate resolution, typically 8-12 bits). The upconversion operation is provided by

$$y(n) = x_i(n)\, s_1(n) + x_q(n)\, s_2(n) \qquad (2)$$

where $s_1(n)$ is the signal $\{1,1,-1,-1,\ldots\}$ and $s_2(n)$ is the signal $\{-1,1,1,-1\ldots\}$. Here we use the fact that $f_s=4\ f_o$. The resultant signals are then passed into a digital band-pass delta-sigma modulator. This BPDS modulator comprises one or more digital resonators, a single-bit quantizer, a dither source, and a feedback loop, in which the output bit is fed back to the input. The overall structure of a representative BPDS modulator is depicted in Fig. 1 (inset). Resonators in the BPDS modulator can be implemented in a variety of ways, but a particularly simple realization is based on the fact that the center frequency of the resonator is $f_o= f_c/4$. DSP operations can be carried out without multiplies.

Calculated frequency spectra corresponding to a representative IS-95 CDMA signal with 1.22MHz bandwidth, the upconverted signal with 900MHz center frequency, the BPDS output signal, and the transmitted signal after filtering, are shown in Fig. 2. The BPDS output signal has significant quantization noise, which is shaped out of band. The maximum input signal that this particular BPDS modulator can successfully pass with high signal to noise ratio depends on the amplitudes and types of signals used to drive it. For this particular CDMA signal, the maximum input power has been determined by simulation to be approximately 15% of the quantizer

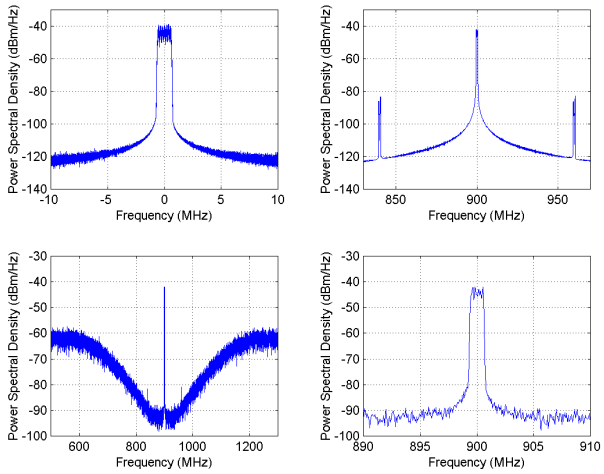

Fig. 2: Computed power spectral densities for upconversion and BPDS encoding of CDMA signal.

output power.

The BPDS output signal can be used to drive a switching mode power amplifier. It has been shown experimentally that good efficiency (>50% drain or collector efficiency) coupled with good linearity (IM3 levels of 40dBc or better) are possible with such amplifiers. To date, these demonstrations have been done at a relatively low output frequency (10MHz) [2,4]. However, simulations suggest that efficient operation at higher frequencies is possible [1,3].

The analog output filter of the system requires careful design. In addition to removing undesired spectral components from the output, the filter recycles power associated with those components back to the switching transistor, so that they do not increase power consumption.

In order to achieve high dynamic range for the transmitter output, it may be worthwhile to scale the I and Q input signals such that their peak values are of the order of the maximum input swing appropriate for the BPDS modulator. The output of the switching mode power amplifier can be modulated by the resulting scaling factor via control of the power supply voltage with a digitally controlled dc-dc converter.

III. EXPERIMENTAL TECHNIQUE AND RESULTS

To experimentally demonstrate the digital bit signals encoding wireless communications signals, a computer-generated bit stream was computed (using MATLAB) and stored in a logic analyzer. The digital signals could be read out (in a repetitive fashion) at a rate of up to (and beyond) 200Mb/S per channel (limited by the capabilities of the logic analyzer). In order to demonstrate signals in the cellular band, a digital 16:1 serializer was used to combine the data of 16 separate channels. A block diagram of the experimental system is shown in Fig. 3. The serializer used was a Conexant CX60061 chip implemented in GaAs HBT technology. The serializer output was a digital signal at 3.6Gb/S. A representative eye diagram is shown in Fig. 4.

After programming the logic analyzer with an appropriate dataset corresponding to a CDMA IS-95 signal, the output data stream was measured with a spectrum analyzer. Fig. 5 shows representative results, on a fine-grained frequency resolution. The CDMA output signal is visible, and the background noise in the cellular band is low. The figure shows schematically the limits on spurious power for the transmitter in the adjacent and alternate channels imposed by the IS-95 specifications.

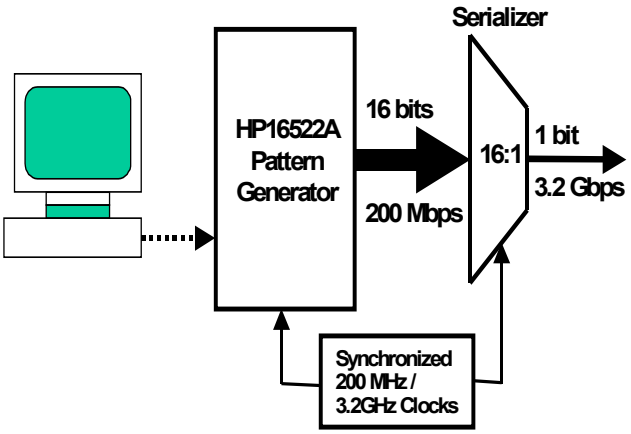

Fig. 3: Experimental system used to generate digital data streams encoding the RF signals.

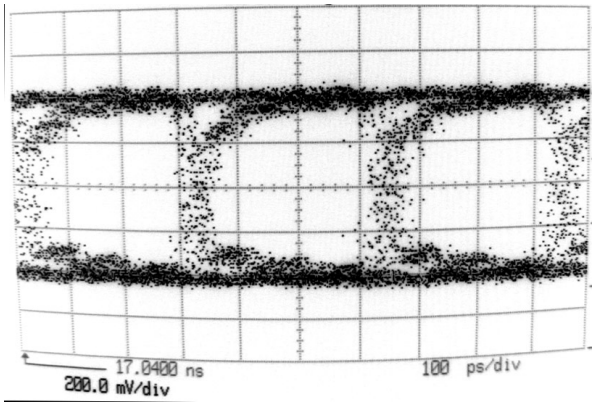

Fig. 4: Measured eye diagram of output digital signals (100pS per division).

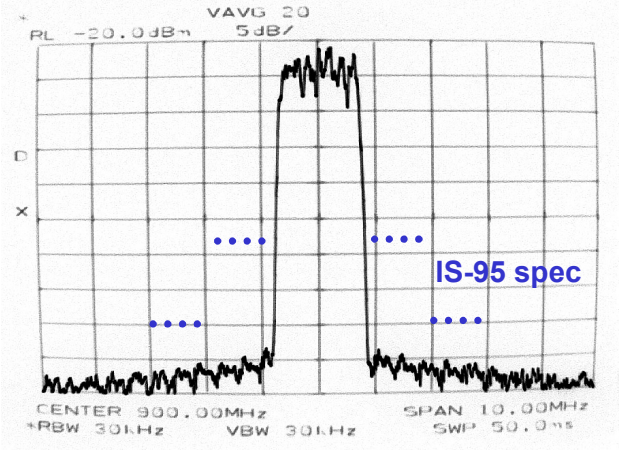

Fig. 5: Output spectrum for CDMA signal, span 10 MHz, 5 dB/div vertical scale. The limits for adjacent and alternate channel power for IS-95 signals are shown.

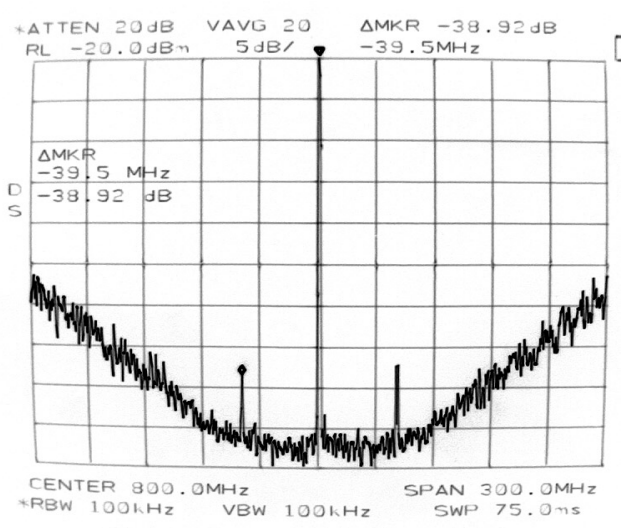

Fig. 6: Measured output spectrum (span 100 MHz, 5 dB/div vertical scale).

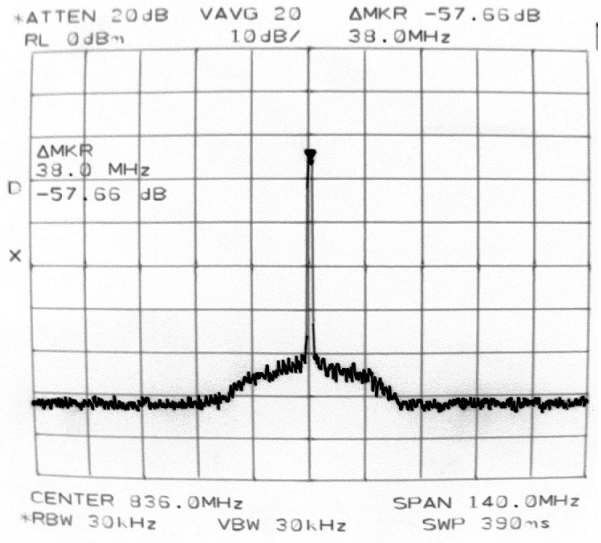

Fig. 7: Measured output spectrum after filtering (span 140 MHz, 10 dB/div vertical scale).

The digital signal is well within the bounds of the specification. Fig. 6 shows the same signal over a broader frequency range. The quantization noise can be seen to increase away from the center frequency, as expected from the noise shaping process. Also visible are two peaks that correspond to incompletely suppressed images of the data signal produced during the upconversion process. The out of band noise can be suppressed from the output by passive analog filtering. As described above, one goal of the filtering is to recycle the majority of the out of band power, so that it does not degrade the overall power efficiency of the system. One of the important challenges in filtering is the removal of spurious power from the channels corresponding to the receiver for the case of FDD (frequency division duplex) systems, in which the transmitter and receiver simultaneously operate. The use of filters with sharp characteristics (such as the ceramic filters used in present CDMA technology) must be used. Fig. 7 shows the output spectrum after passing the signal through a Toko four pole dielectric filter. In this figure, the noise floor of the spectrum analyzer masks the filter suppressed quantization noise in the receive band.

V. CONCLUSION

An architecture has been presented that has the potential for the integration of the circuitry associated with an RF transmitter into a single DSP-based IC, used together with a switching mode power amplifier and an analog filter. The integration of the transmitter offers potential advantages of minimizing component drift and need for adjustment, lower parts count and size, and easier assembly. The use of band-pass delta-sigma signals eliminates the need for a high resolution DAC, and enables the use of switching mode amplifiers, which have the potential for increasing efficiency. The architecture offers the potential for easy reprogrammability of the transmitter function, since the DSP could in principle be used in different ways without changing hardware.

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